ABSTRACT OF THE DISCLOSURE

An erasing method for the memory cells of a non-volatile memory is provided. Each memory cell comprises a gate, a source, a drain, an electron-trapping layer and a substrate. The data within the memory cell is erased by applying a first voltage to the control gate, applying a second voltage to the source, applying a third voltage to the drain and applying a fourth voltage to the substrate. The electrons are pulled from the electron-trapping layer into the channel by negative gate F-N tunneling effect.